Ebullient Cooling of Electronics: Future Trends and Recent Advances

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Despite the precipitous drop in transistor switching energy that has characterized the solid-state semiconductor revolution, the cooling requirements of microelectronic components have not diminished. As the 21st century begins, high performance chip power dissipation exceeds 100 W, and informed opinion suggests that power dissipation will continue rise over the rest of the present decade. Thermal management is thus one of the key challenges in advanced electronic packaging and considerable improvement in thermal packaging will be needed to successfully exploit the "Moore's Law" acceleration in semiconductor technology.

In the late 1990's, under the influence of market forces, thermal management of nearly all the products in the "*High Performance*" category devolved to the aggressive use of air cooling, exploiting technology that was a natural outgrowth of the air-cooled multi-chip modules of the 1980's. Thus, by the end of the decade, a renaissance in thermal packaging produced heat sinks for high-end commercial workstations and servers that were routinely dissipating 60-70 W, with chip heat fluxes of some 26 W/cm^2. The packaging community consensus suggests that early in the second decade of this century power dissipation will rise to 175 W for chips operating at some 3 GHz. It is anticipated that chip area, growing from 3.8 cm^2 to some 7.5 cm^2, will keep pace with chip power dissipation in the coming years, yielding average chip heat fluxes that increase only marginally above the present values to approximately 30 W/cm^2 by 2006, before beginning a slow decline in later years.

Cost-effective thermal management of large silicon chips with power dissipation approaching 200 W requires exploration of non-conventional thermal packaging techniques, including direct cooling with dielectric liquids. The high dielectric strength and low dielectric constant of these liquids, as well as their chemical inertness, make it possible to immerse most electronic components directly in these fluorochemical liquids (PFCs and Novec fluids). Pool boiling on the chip surface transfers the dissipated heat directly into the liquid and, thus, overcomes the barrier posed by the interface resistance otherwise encountered at the solid interface between the chip and the cooling hardware. With saturated pool boiling, component heat fluxes in the range of 10 - 20 W/cm^2 could be removed at surface superheats of typically less than 20 K.

The critical heat flux (i.e. CHF), places an upper limit on this highly efficient heat transfer process. Heat fluxes in excess of CHF result in the formation of an insulating film of vapor on the heat transfer surface and superheats typically higher by an order-of-magnitude than encountered in nucleate pool boiling. Most predictive models for pool boiling CHF are based on the analysis of hydrodynamic phenomena leading to the "choking off", or interruption, of the liquid supply to the heater. The course discussions will be on;

- The fundamentals of the boiling heat transfer and CHF
- Dielectric liquids
- Effects on the CHF (pressure, subcooling, surface treatments, binary mixtures, thermal effusivity etc)
- Discussions on the practical examples of passive cooling schemes, and several active cooling designs